Journal of Ceramic Processing Research. Vol. 9, No. 3, pp. 282~285 (2008)

J O U R N A L O F
Ceramic
Processing Research

Field effect transistor properties of ZnO nanowires

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Zinc oxide (ZnO) nanostructures were grown on Si (001) substrates by thermal chemical vapor deposition without any catalysts. The deposition temperatures varied from 800 °C to 1100 °C. SEM and XRD data suggest the nanostructures are well-aligned, single ZnO crystals with a (0002) preferential orientation. Back-gate ZnO nanowire field effect transistors (FET) were also successfully fabricated using a photolithography process. The fabricated nanowire FET exhibited Ohmic contact between the ZnO nanowire channels and Au metal electrodes. The ZnO nanowire exhibited n-type field effect transistor behavior denoted by an increase in current with increasing gate voltage.

Key words: Thermal CVD, Zinc Oxide, Nanostructures, and FET.

Introduction

Zinc oxide (ZnO) has: a hexagonal structure, lattice constants of a = 0.324-0.326 nm and c = 0.513-0.543 nm, a wide band-gap of 3.37 eV, and a large exciton binding energy of 60 MeV at room temperature [1-3]. The synthesis of semiconducting, nanostructure materials has been carried out in graphitic nanotubes [4]. Compound semiconducting nanomaterials including GaN [5], GaP [6], InP [7], ZnO [8, 9], and Ga_2O_3 [10] have also been developed for the fabrication of nano-optoelectronic devices. ZnO has been attracting considerable attention for such optoelectronics applications as transparent thin film transistors (TFT), field effect transistors (FET), and ultraviolet light emitting devices (LED). A light emitting diode of a single ZnO crystal is expected to have high energy efficiency due in part to its intense band edge luminescence upon laser excitation [11] and its photoluminescence (PL) spectrum showing blue emission at 380 nm. In particular, the electronic properties of semiconductor surfaces are strongly affected by the chemical adsorption of ambient gases [12-15]. Wide band-gap nanowires have attracted much interest owing to their remarkable chemical and physical properties [16]. High quality polycrystalline ZnO nanowires prepared by thermal CVD on silicon substrate have been reported [1-3, 8, 9].

The interest in field effect transistors (FET) has drastically increased over the past few years and extensively studied for many potential applications ranging from displays and identification tags to sensors [17]. In particular, the application of nanowires to FET has been intensely researched due to the various advantages nanowires have, including good transportation of charge and high crystalline quality [18]. Currently, photolithography employing ZnO nanowire FETs based on back-gate structures is used to fabricate many nanowire FETs. In integrated devices, it is impossible to individually control each back-gate FET [19]. In this study, a fabrication technique is developed for back-gate nanowires FETs using photolithography. The electrical properties of the top- and back-gate ZnO nanowire FETs are characterized by conventional *I-V* measurements.

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Experimental

ZnO nanowires were grown on silicon substrates using thermal chemical vapour deposition (CVD). ZnO nanowires were synthesized by thermally vaporizing a mixture of commercial ZnO powder (99.999%) and graphite powder (99%) in a 1:1 ratio in a quartz tube furnace with silicon (100) as the substrate for nanowire growth. The Si substrate (10 mm × 10 mm) was placed facedown on an aluminum, ceramic boat loaded with a mixture of the powders at a thickness of approximately 2 mm. The boat [15 mm × 15 mm × 400 mm] was inserted into the tube of the quartz furnace under a constant flow of argon (40 sccm) and oxygen (20 sccm) and heated up to 800-1100 °C for 30 minutes. Figure 1 shows a schematic of the Thermal CVD system used for the deposition of the ZnO nanowires. No catalyst was utilized in any of the deposition processes.

To fabricate the ZnO nanowire FET device, ZnO nanowires grown on the Si substrate were transferred from the substrate to a silicon wafer using a 500 nm thick, thermally grown oxide, made by dropping a nanowire suspension in water. The nanowire suspension was made

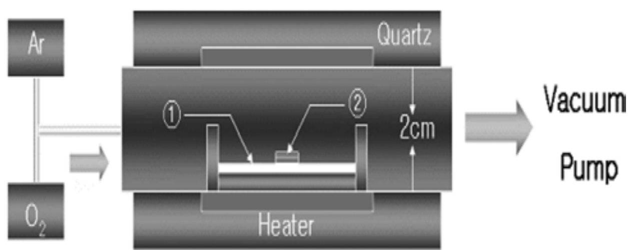

Fig. 1. Schematic diagram of the thermal CVD system (① : ZnO + Graphite powder, ② : Silicon substrate).

by brief sonication of the substrate with ZnO nanowires on its surface in water for 10-20 s. Maker patterns were fabricated in order to indicate the position of the nanowires and to serve as alignment makers. First, a photoresist layer was spin-coated on a maker Si (100) substrate. Second, the photoresist layer was fabricated using a photolithography process employing a lift-off process using a PR remover solution [20, 21]. Finally, metal electrodes consisting of Ti (4 nm)/Au (12 nm) were deposited by an evaporator, giving a final distance of 1-2 μm between the source and drain electrode.

The crystalline phases of the thin films were identified by an X-ray diffractometer (Scintag SDS 2000) while microstructure and surface roughness were observed by a field emission scanning electron microscope (Hitachi S 2500C). The electrical properties of the FET were studied at room temperature by a prove station (national instrument).

Results and Discussion

Figure 2 shows scanning electron microscopy (SEM) images of ZnO nanostructures grown at substrate temperatures of 800, 900, 1000, and 1100 °C. The deposition rate was approximately 288 nm/minute at 1100 °C. One distinctive feature of the wires in Fig. 2, compared with other nanowires obtained by catalyst-assisted growth reported elsewhere, is their sharp tips Fig. 2(c), which seem to be characteristic of catalyst-free growth. In the experimental process, Fig. 2(a) and 2(b) demonstrate that micromaterials synthesized on the Si substrate are mixtures of micro and bulk, due in part to the small amounts of the ZnO powder source. Fig. 2(d) shows the mean diagonal lengths and mean heights of these nanowires measured to be approximately 60 and 500 nm, respectively, giving an aspect ratio of approximately 8. Figure 3(a) shows the XRD diffraction patterns of ZnO nanowires grown at a substrate temperature of 1100 °C. Based on these XRD analyses, the nanowires are single crystalline in nature and consist of a single phase of ZnO with a hexagonal structure. The nanowires grown at 1100 °C also have good crystallinity with a sharp (0002) major peak. Figure 3(b), the PL spectrum of the ZnO nanowires, shows a single near-band emission peak at approximately 530 nm with an observed dominant near-band edge emission peak at 3.29 eV and a main peak green emission at 2.31 eV. The green band emission from the ZnO nanostructure is generally explained as a hole with an electron in a singly ionized oxygen vacancy [22]. Figure 3(c) is a typical bright field TEM image of a nanowire and a lattice distance is 0.2 nm in which the nanowire is smooth and clean on the surface and the SAED Fig. 3(d) pattern clearly exhibits visible dark spots that correspond to the crystal planes of the hexagonal ZnO. Hence, it is confirmed that single crystal nanowires having good crystalline qualities can be grown without a catalyst via an epitaxial growth technique.

Figure 4(b) shows a SEM image of the ZnO nanowires between the source and drain electrode. A heavily doped P-type Si substrate was utilized as the back-gate electrode. The channel length between the source and drain electrodes

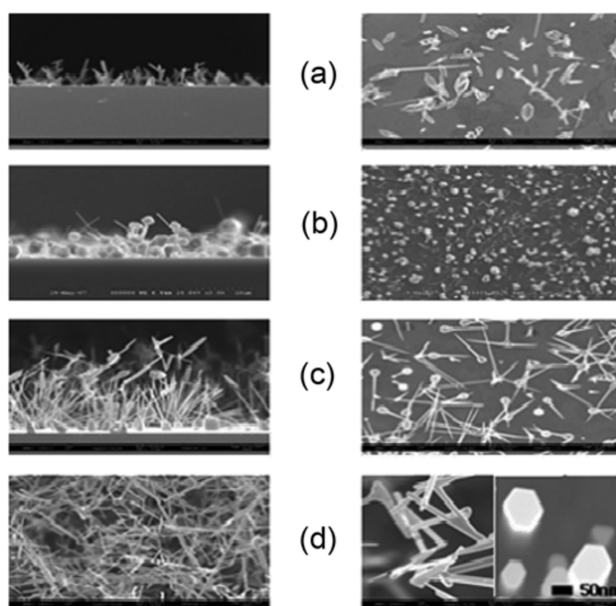

Fig. 2. Cross-sectional and surface SEM images of ZnO nanowires as a function of deposition temperatures : (a) 800 °C, (b) 900 °C, (c) 1000 °C and (d) 1100 °C.

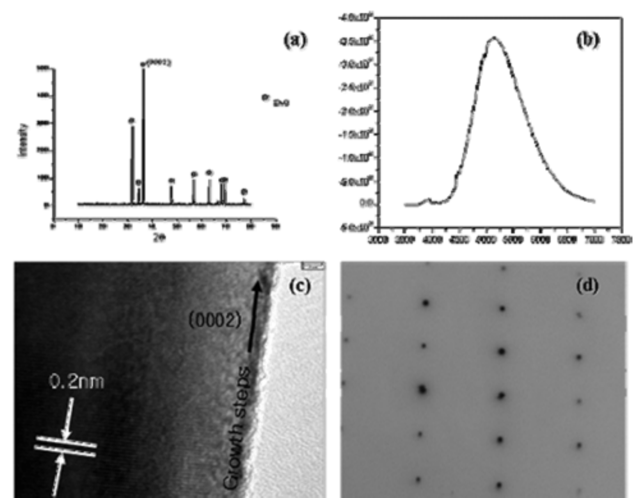

Fig. 3. (a) the XRD diffraction patterns of ZnO nanowires. (b) PL emission spectrum showing a strong emission at approximately 530 nm. (c) HRTEM image of an individual ZnO nanowire showing its [0002] growth direction. (d) SAED of ZnO nanowires.

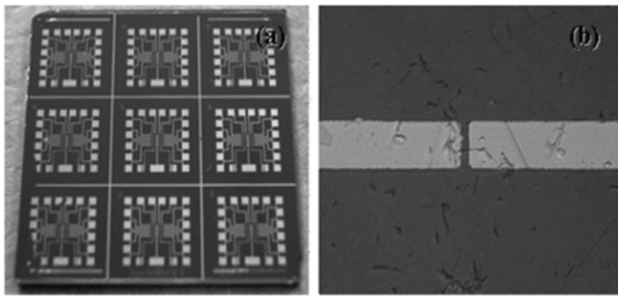

Fig. 4. (a) Real picture of Mask pattern, (b) SEM image of ZnO nanowire between source and drain.

is 1 μm and the thickness of the SiO_2 gate oxide layer is 500 nm. We evaluated the device performance of the back-gate nanowire FET fabricated by the photolithography process. Figure 5(a) shows the Ids-Vds curves of the back-gate FET for Vg ranging from −1 V to 1 V. The drain voltage and slopes of the Ids-Vds curves are dependent on the gate voltage, revealing the ZnO nanowire channel to be n-type. As shown in Fig. (5), the ZnO nanowire FET exhibits typical n-type semiconducting behavior since the current increases with increasing positive gate voltage, whereas it decreases down to a few picoamperes with increasing negative gate voltage. It is well known that undoped ZnO generally exhibits n-type conduction due to the presence of intrinsic donor-type defects induced by deviation from stoichiometry [23]. The linear characteristic of the Ids-Vds curves shows there is Ohmic contact between the ZnO nanowire channel and the Au metal electrodes. In Fig. 5(b), within the Ids-Vg curve, the drain current Ids increases as the gate voltage, Vg, varies from −10 V

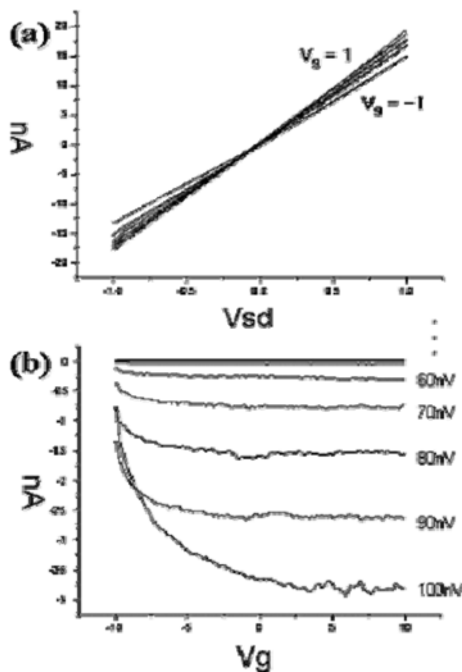

Fig. 5. (a) Ids-Vds curves of the back-gate FET for Vg ranging from −1 V to 1 V (b) Ids-Vg curves.

to +10 V. The oxide capacitance of the back-gate FET was found to be 3.71×10^{-11} F from the equation,

$$C = 2\pi\varepsilon_r\varepsilon_0 L/\ln(2h/r) \ [24] \quad (1)$$

where ε_r is the dielectric constant of SiO_2 (3.9), L the gate length (1 μm), h the thickness of SiO_2 (500 nm), r the radius of the nanowire (60 nm), and ε_0 is 8.85×10^{-12}.

Conclusions

In summary, we have demonstrated the catalyst-free synthesis of ZnO nanowires on an Si (100) substrate by thermal CVD. The ZnO nanowire was a single crystal with a hexagonal structure and a preferred growth (0002) direction. The nanowires had an average diameter of 60 nm and an average length of 500 nm. We were also able to fabricate a back-gate ZnO nanowire FET by a photolithography process, yielding an FET exhibiting ohmic (semiconductor + conductor) contact between the ZnO nanowire channel and the Au metal electrode. The ZnO nanowire exhibited a n-type field effect transistor behavior denoted by an increase in current with increasing gate voltage.

Acknowledgements

"This work was supported by the Korea Research Foundation Grant funded by the Korean Government (MOEHRD)" (The Regional Research Universities Program/ Chungbuk BIT Research-Oriented University Consortium).

References

1. C.-J. Lee, T.-J. Lee, S.-C. Lyu and Y. Zhang, Appl. Phys. Lett. 81 (2002) 3648-3650.
2. J.-S. Lee, M.-I. Kanga, S. Kim, M.-S. Lee and Y.-K. Lee, J. Cryst. Growth 249 (2003) 201-207.
3. H.-J. Yuan, S.-S. Yuan, D.-F. Liu, X.-Q. Yan, Z.-P. Zhou, L. Ci, J. Wang, Y. Gao, L. Song, L.-F. Liu, W.-Y. Zhou and G. Wang, Chem. Phys. Lett. 371 (2003) 337-341.
4. N. Hamada, S. Sawada and A. Oshiyama, Phys. Rev. Lett. 68[10] (1992) 1579-1581.
5. W. Han, S. Fan, Q. Li and Y. Hu, Science. 277[5330] (1997) 1287-1289.
6. W.-S. Shi, Y.-F. Zheng, N. Wang, C.-S. Lee and S.-T. Lee, Chem. Phys. Lett. 345[5-6] (2001) 377-380.
7. X. Duan, Y. Huang, Y. Cui, J. Wang and C.-M. Lieber, Nature 409[6816] (2001) 66-69.
8. Z.-W. Pan, Z.-R. Dai and Z.-L. Wang, Science 291[5510] (2001) 1947-1949.
9. M.-H. Huang, Y. Wu, H. Feick, N. Tran, E. Weber and P. Yang, Adv. Mater. 13[2] (2001) 113-116.
10. H.-Z. Zhang, Y.-C. Kong, Y.-Z. Wang, X. Du, Z.-G., Bai, J.-J. Wang, P.-D. Yu, Y. Ding, Q.-L. Hang and S.-Q. Feng, Solid State Communication 109[11] (1999) 677-682.
11. M. Kawasaki, A. Ohtomo, I. Ohkubo, H. Koinumal, Z.-K. Tang, P. Yu, G.-K.-L. Wong, B.-P. Zhang and Y. Segawa, Mat. Sci. Eng. B56 (1998) 239-245.
12. J.-B. Baxter and E.-S. Aydil, Appl. Phys. Lett. 86, 053114 (2005) 1-3.

13. W. Monch, J. Vac Sic. Technol. 7 (1989) 1216-1219.
14. A. Many, Y. Goldstein and N.-B. Grover, Semiconductor Surfaces, North-Holland, Amsterdam, 1965.
15. W. Monch, Semiconductor Surface and Interfaces, 3rd ed., Springer, Berlin (2001).
16. Y. Cui, Q. Wei, H.-K. Park, and C.-M. Lieber, Science 293 (2001) 1289-1292.
17. C. Dimitrakopoulos and P.-R.-L.-M. Malenfant, Adv. Mater. 14 (2002) 99-99.
18. J. Hu, T.-W. Odom and C.-M. Lieber, Acc. Chem. Res. 32 (1999) 435-445.
19. S. Ju, K. Lee, D.-B. Janes, M. Yoon, A. Facchetti and T.-J. Marks, Nano Lett. 5 (2005) 2281-2286.
20. K. Keem, J.-M. Kang, C.-J. Yoon, D.-H. Yeom, D.-Y. Jeong and B.-M. Moon, Micro. Eng. 84 (2007) 1622-1626.
21. W.-K. Hong, B.-J. Kim, T.-W. Kim, G.-H. Jo, S.-H. Song and S.-S. Kwon, Colloids and Surfaces A 313-314 (2007) 378-382.
22. K. Vanhausden, W.-L. Warren, C.-H. Seager, D.-R. Tallant, J.-A. Voigt and B.-E. Gande, J. Appl. Phys. 79 (1996) 7983-7990.
23. D.-C. Look, J.-W. Hemsky and J.-R Sizelove, Phys. Rev. Lett. 82 (1999) 2552-2555.
24. Y. Huang, X. Duan, Y. Cui and C.-M. Lieber, Nano Lett. 2 (2002) 101-104.