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Comparison of phonon-limited electron mobility in strained Si grown on silicon on insulator (sSOI) and SiGe on insulator (SGOI)

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Through theoretical calculation, the phonon-limited electron mobility in fully depleted strained Si n-channel MOSFETs fabricated on silicon on insulator (i.e., sSOI) and SiGe on insulator (SGOI) was compared between the two structures as a function of Si thickness. In the Si thickness range from 10 nm down to 3 nm, the phonon-limited electron mobility in the sSOI n-MOSFET was about 1.5 times higher than that of a conventional SOI n-MOSFET. In particular, it was found that the electron mobility in the sSOI n-MOSFET was about 3% lower than that in the SGOI n-MOSFET. This difference can be attributed to two physical phenomena: first, that the sSOI n-MOSFET has higher inter-valley scattering rates than does the SGOI n-MOSFET, because of its greater carrier confinements: and second, that some electrons in the inversion layer of the SGOI n-MOSFET tunnel into the SiGe layer. These theoretical results are strongly consistent with previous experimental results.

Key words: Strained Silicon, sSOI n-MOSFET, Ultra-thin Body, Electron Mobility Enhancement.

Introduction

As conventional scaling laws become less effective in boosting semiconductor device performance for 90-nm and smaller complementary metal-oxide-semiconductor field-effect transistor (CMOSFET) technologies, substrate structural engineering is playing an increasing role in enhancing performance. Strained silicon has drawn much attention because of its enhanced electron and hole mobilities and its compatibility with main stream Si MOS processing [1-5]. Recently, there have been numerous efforts to fabricate strained silicon with a silicon-on-insulator (SOI) structure in order to utilize SOI-specific benefits, such as a dual gate possibility [6-7], reduced parasitic capacitance, and improved device scaling. Most of these performance enhancement approaches have utilized the formation of relaxed SiGe on insulator (SGOI) to induce a tensile strain in the top Si. Unfortunately, the relaxed SiGe layer in the structure creates several CMOS process compatibility issues, including germanium out-diffusion into the strained Si [8], formation of low-resistance silicide, and altered dopant diffusion [9-10]. To overcome these process issues, strained Si grown on an SOI structure (i.e., sSOI) has been investigated. This approach would provide compatibility with conventional CMOS processes in mass production by eliminating the SiGe layer and thus avoiding the formation of Si surface defects caused by threading dislocations induced by the lattice mismatch between Si and SiGe [11-12].

So far, although several reports demonstrating performance enhancement with sSOI n-channel MOSFETs have been published, it has not yet been confirmed which structure is more effective from the viewpoint of current transports when the top strained Si layer is thinner than 10 nm. In this study, therefore, we theoretically simulated and compared the electron mobility in strained Si grown on silicon-on-insulator (i.e., sSOI) and SiGe-on-insulator (SGOI). We also considered the quantum mechanical (Q.M) model in order to speculate which structure would be more effective in the Si thickness range of below 10 nm. In particular, we analyzed the electronic states of both the two- and four-fold valleys, including such characteristics as the energy band diagram, the electron occupancy, the electron concentration, the phonon scattering rate, and the phonon-limited electron mobility.

Experiments

To investigate the dependency of the phonon-limited mobility on strained Si thickness, we began by extracting the phonon-limited mobility by the relaxation time approximation method [13-14], implemented by solving the 2D Poisson and 1D Schrodinger equations self-consistently.

First, the momentum-relaxation rate [13-14] for deformation potential scattering by intra-valley acoustic phonons from the ith sub-band to the jth sub-band, is

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given by the following equations:

$$\frac{1}{\tau_{ac2}^{i,j}} = \frac{n_{v2}^{ac} m_d D_{ac}^2 k_B T}{\hbar^3 \rho s_l^2}\frac{1}{W_{i,j}}, \tag{1}$$

$$W_{i,j} = \{\int \xi_i^2(z)\xi_j^2(z)dz\}^{-1}, \tag{2}$$

$$\frac{1}{\tau_{ac4}^{i,j}} = \frac{n_{v4}^{ac} m_d D_{ac}^2 k_B T}{\hbar^3 \rho s_l^2}\frac{1}{W_{i,j}}, \tag{3}$$

$$W'_{i,j} = \{\int \xi'^2_i(z)\xi'^2_j(z)dz\}^{-1}, \tag{4}$$

where n_{v2}^{ac} is the degeneracy of the valley with respect to intra-valley scattering, m_d is the density-of-state mass in each valley, D_{ac} is the deformation potential due to acoustic phonons, ρ is the crystal density, and S_l is the sound velocity. $W_{i,j}$ is interpreted as the effective thickness of the wave function of the ith sub-band with respect to z [15].

Second, the inter-valley phonon scattering rate can be obtained from the following four equations. The momentum-relaxation rate [13-14], for inter-valley phonon scattering from the ith sub-band to the jth sub-band is given by

$$\frac{1}{\tau_{\text{inter2}}^{i,j}} = \sum_k^{\{f\}} \frac{n_{v2\to4}^{f} m_{d4} D_4^2}{\hbar \rho E_k}\frac{1}{V_{i,j}}\left(N_k+\frac{1}{2}\pm\frac{1}{2}\right)\left(\frac{1-f(E\mp E_k)}{1-f(E)}\right), \tag{5}$$

$$\frac{1}{\tau_{\text{inter4}}^{i,j}} = \sum_k^{\{f\}} \frac{n_{v4\to4}^{f} m_{d4} D_k^2}{\hbar \rho E_k}\frac{1}{W'_{i,j}}\left(N_k+\frac{1}{2}\pm\frac{1}{2}\right)\left(\frac{1-f(E\mp E_k)}{1-f(E)}\right), \tag{6}$$

$$\frac{1}{\tau_{\text{inter4}}^{i,j}} = \sum_k^{\{g\}} \frac{n_{v4\to4}^{f} m_{d4} D_k^2}{\hbar \rho E_k}\frac{1}{W'_{i,j}}\left(N_k+\frac{1}{2}\pm\frac{1}{2}\right)\left(\frac{1-f(E\mp E_k)}{1-f(E)}\right), \tag{7}$$

$$\frac{1}{\tau'^{i,j}_{\text{inter4}}} = \sum_k^{\{f\}} \frac{n_{v4\to2}^{f} m_{d2} D_k^2}{\hbar \rho E_k}\frac{1}{V'_{i,j}}\left(N_k+\frac{1}{2}\pm\frac{1}{2}\right)\left(\frac{1-f(E\mp E_k)}{1-f(E)}\right), \tag{8}$$

where $n_{v4\to4}^{f}$ (=4) is the degeneracy of the valley into which the electrons are scattered; D_k and E_k are the deformation potential and energy, respectively, of the kth inter-valley phonon; N_k is the occupation number of the kth inter-valley phonon; the plus and minus signs in the expression (N_k+1/2±1/2) correspond to phonon emission and phonon absorption, respectively; and $f(E)$ is the Fermi-Dirac distribution function; and $n_{v2\to4}^{f}$, $n_{v4\to4}^{g}$, and $n_{v4\to2}^{f}$ are the degeneracies of the valleys into which the electrons are scattered, and are taken as 2, 1, and 2, respectively. To provide the parameters for inter-valley phonon scattering, we applied the Ferry model [14]. We considered only equivalent inter-valley scattering, i.e., from X valley to X valley, rather than from X valley to L valley.

The total relaxation times, $\tau_2^i(E)$ and $\tau_4^i(E)$, for electrons with energy E in the ith sub-band of the two- and four-fold valleys, respectively, are given by

$$\frac{1}{\tau_2^i}(E) = \frac{1}{\tau_{ac2}^i}(E)+\frac{1}{\tau_{\text{inter2}}^i}, \tag{9}$$

$$\frac{1}{\tau_4^i}(E) = \frac{1}{\tau_{ac4}^i}(E)+\frac{1}{\tau_{\text{inter4}}^i}. \tag{10}$$

By using Matthiessen's equation, the carrier mobility in a longitudinal field can be described approximately as the sum of three scattering terms [16-17]:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_c}+\frac{1}{\mu_{ph}}+\frac{1}{\mu_{sr}}, \tag{11}$$

where μ_c is the Coulomb scattering mobility, μ_{ph} is the phonon-limited mobility, μ_{sr} is the surface roughness mobility, and μ_{eff} is the effective mobility. Among the three mobility components, we only considered the phonon-limited electron mobility for the conventional SOI and SGOI structures as described above.

The electron mobilities of the two-fold and four-fold valleys are given by the following equations:

$$\mu_2^i = \frac{e\int_{E_i}^{\infty}(E-E_i)\tau_2^i(E)(-\partial f/\partial E)dE}{m_{c2}\int_{E_i}^{\infty}(E-E_i)(-\partial f/\partial E)dE}, \tag{12}$$

$$\mu_4^i = \frac{e\int_{E_{i'}}^{\infty}(E-E_i')\tau_2^i(E)(-\partial f/\partial E)dE}{m_{c4}\int_{E_{i'}}^{\infty}(E-E_i')(-\partial f/\partial E)dE}, \tag{13}$$

where m_{c2} and m_{c4} are the conductivity masses of the two- and four-fold valleys, respectively. The total electron mobility is given by

$$\mu = \left(\sum_i \mu_2^i N_i + \sum_{i'} \mu_4^{i'} N_{i'}\right)(N_s)^{-1}, \tag{14}$$

where μ_2^i and μ_4^i are the respective mobilities for electrons in the ith sub-band of the two- and the four-fold valleys, and N_s is the total surface carrier concentration in the inversion layer.

To investigate the dependency of the phonon-limited electron mobility on the thickness of the strained inversion layer, we varied the strained Si thickness (T_{Si}) on the relaxed SiGe layer, which had a Ge concentration of 20 at%, as depicted in Fig. 1. The strained Si layer was p-type (100) and had a doping concentration of 1.5 $\times 10^{15}$ cm^{-3}.

Result and Discussion

Simulating the electronic states in the sub 10-nm strained Si layer of the SGOI n-MOSFET requires an accurate scattering model. Although theoretical work on the electron mobility have been published, no mobility comparison of sSOI and SGOI n-MOSFET structures has been published yet. Thus, we modified and optimized the parameters of the mobility model

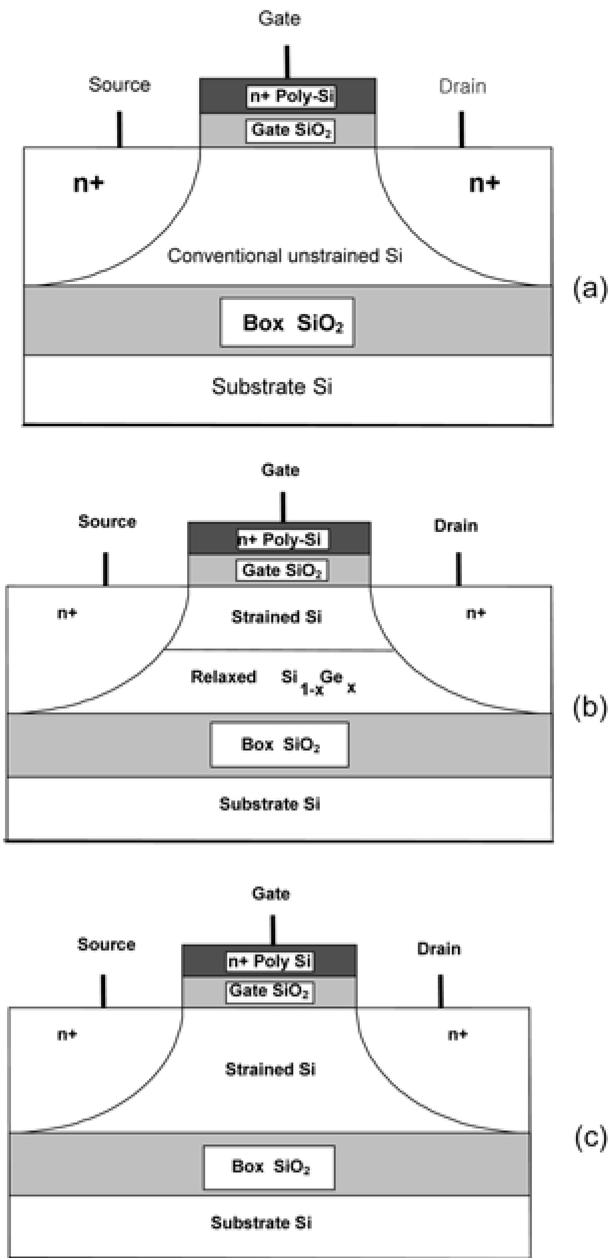


Fig. 1. Schematic diagram illustrating the structure of (a) an unstrained SOI n-MOSFET and (b) a strained SGOI n-MOSFET, and (c) an sSOI n-MOSFET.

based on a bulk-Si MOSFET. Utilizing a numerical simulator coded in C, we extracted the phonon-limited electron mobility curve as a function of the Ge mole fraction, under the condition of 1.5-V gate bias, as shown in Fig. 2. The figure includes both previous experimental data and the calculated curve obtained in our simulation, showing reasonable consistency. In particular, it is notable that the mobility enhancement ratio for an sSOI n-channel MOSFET reported by Yin et al. [10] precisely agreed with our simulated curve.

Figure 3 shows the wave function of the ground state under a 1.5-V gate bias condition, drawn on an energy band diagram, for (a) a 5-nm-thick strained Si layer in

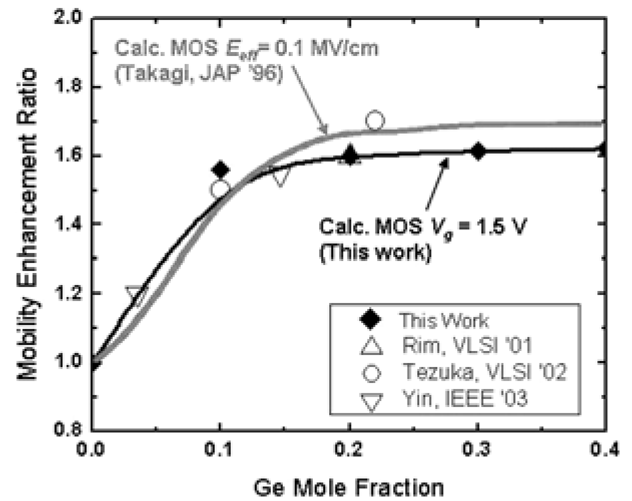
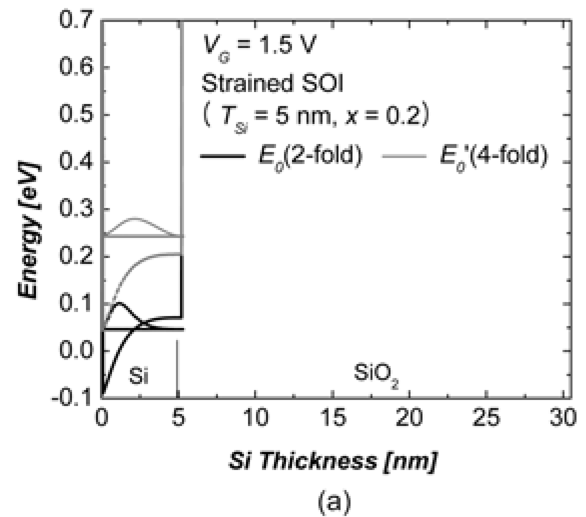


Fig. 2. Comparison of the mobility enhancement as a function of the substrate Ge fraction, including both experiment data and a calculated curve from the simulation.



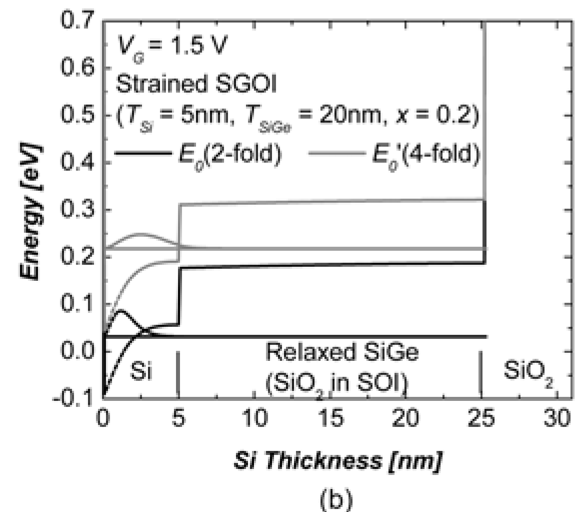


Fig. 3. Electron probability of the ground state under a 1.5-V gate bias condition, for (a) a 5-nm-thick sSOI n-MOSFET induced by a 20-at% Ge concentration and (b) an n-MOSFET with 5 nm of strained Si on 20-nm SiGe on SOI with a 20-at% Ge concentration.

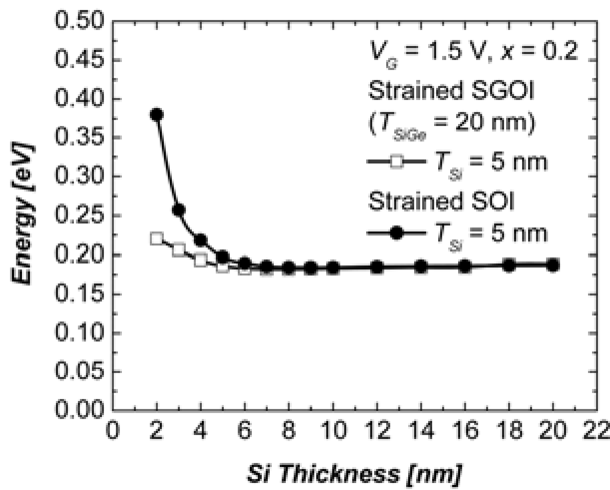


Fig. 4. Energy difference (ΔE) between the ground states of the two-fold (E0) and four-fold valleys (E0') as a function of the Si thickness.

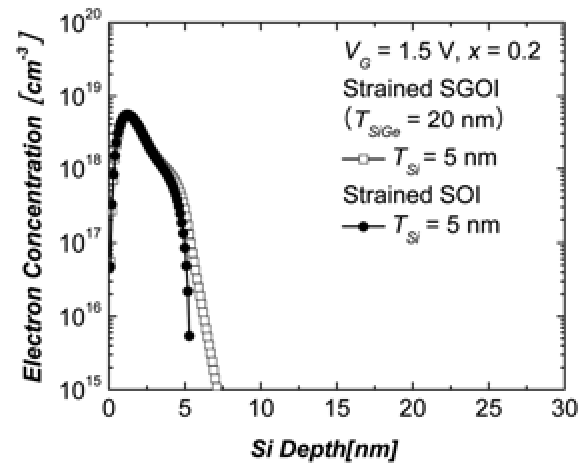


Fig. 5. Electron concentration in the inversion layer as a function of depth below the Si surface under a 1.5-V gate bias condition.

an sSOI n-MOSFET and (b) a 5-nm strained Si layer on a 20-nm SiGe layer with a 20-at% Ge concentration. These results demonstrate that the energy value of the ground state in two-fold valleys for the sSOI n-MOSFET is equal to that for the SGOI n-MOSFET, whereas, the energy for the four-fold valleys is somewhat higher for the sSOI n-MOSFET than for the SGOI n-MOSFET. This difference for the four-fold valleys might result from the fact that the inversion layer in the sSOI n-MOSFET is confined by a potential barrier caused by the buried oxide. In addition, for the corresponding value in the two-fold valleys, the tensile strain induced by the SiGe was assumed to be equivalent.

Figure 4 shows the energy difference (ΔE) of the ground state between the two-fold (E_0) and four-fold valleys (E_0') as a function of the strained Si thickness. The results indicate that as the Si thickness decreases below 6 nm, ΔE for the sSOI n-MOSFET starts to increase abruptly because of a quantum-mechanical effect, while that for the SGOI n-MOSFET increases moderately because of a tunneling effect. It should be noted that when the Si thickness is 6 nm, the ΔE difference between the sSOI and SGOI n-MOSFETs is 0.01 eV, and when the Si thickness is 3 nm, the ΔE difference is 0.05 eV. In other words, a quantum effect occurs in the sSOI n-MOSFET, while a tunneling effect happens in the SGOI n-MOSFET.

Figure 5 shows the electron concentrations as a function of the Si depth below the surface, under a 1.5-V gate bias condition. These results demonstrate that some electrons in the inversion layer of the strained Si SGOI n-MOSFET tunnel into the SiGe layer, while those in the sSOI n-MOSFET were confined by the potential barrier induced by the buried oxide layer, indicating less carrier confinement in the SGOI n-MOSFET than in the sSOI n-MOSFET.

Figure 6 compares the simulated phonon scattering rates of both the sSOI n-MOSFET and the SGOI n-MOSFET with that of a conventional SOI n-MOSFET, including (a) the total phonon scattering rate, (b) the inter-valley scattering rate, and (c) the intra-valley scattering rate. The scattering rate in the sSOI n-MOSFET exhibits a higher value in the electron energy range beyond 3 eV than does the SGOI n-MOSFET. This phenomenon can be considered by examining both the intra-valley and inter-valley scattering rates as shown in Figs. 6(b) and (c). In the case of the intra-valley scattering rates, Fig. 6(c) shows very little difference between the sSOI and SGOI n-MOSFETs as because most of all electrons are populated in the two-fold valleys, whose energy has been lowered. In the case of the inter-valley scattering rates, however, Fig. 6(b) shows that the inter-valley scattering rates in the sSOI n-MOSFET is higher than that in the SGOI n-MOSFET. This is because the electron confinement effect in the sSOI n-MOSFET is greater than that in the SGOI n-MOSFET, resulting that the form factor defined as W and W' in equation (2) and (4) is smaller than that in the SGOI n-MOSFET. In other words, because the effective inversion layer in the sSOI n-MOSFET is narrower than that in the SGOI n-MOSFET. In addition, it should be noted that the comparative amplitude of inter-valley scattering with respect to intra-valley scattering determines the total phonon mobility, so that the total scattering rate depends on the inter-valley scattering rates, rather than on the acoustic intra-valley scattering rates.

Finally, Figure 7 shows the phonon-limited electron mobility as a function of the Si thickness. The electron mobility in both the sSOI n-MOSFET and the SGOI n-MOSFET is about 1.5 to 1.7 times higher than that in the conventional SOI n-MOSFET over the whole range of Si thickness; these results are strongly consistent with previous experimental reports. In addition, we have shown, for the first time, that if the strained Si

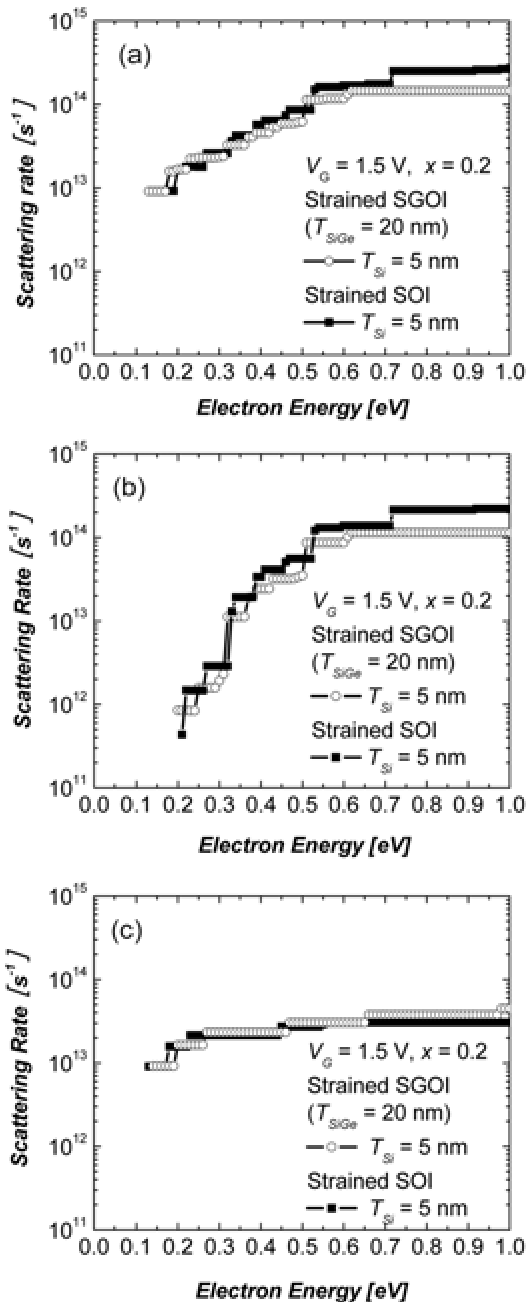


Fig. 6. Simulated phonon scattering rates: (a) the total scattering rate, (b) the inter-valley phonon scattering rate, and (c) the intra-valley phonon scattering rate.

thickness is below 10 nm, the mobility in the sSOI n-MOSFET is 3.2% lower than that in the SGOI n-MOSFET. We attribute this to two cause; (i) the higher inter-valley scattering rates in the sSOI n-MOSFET because of carrier confinement in the narrower inversion layer, and (ii) some electrons in the inversion layer of the SGOI n-MOSFET tunneling into the SiGe layer.

Conclusions

In this paper, we have compared the phonon-limited

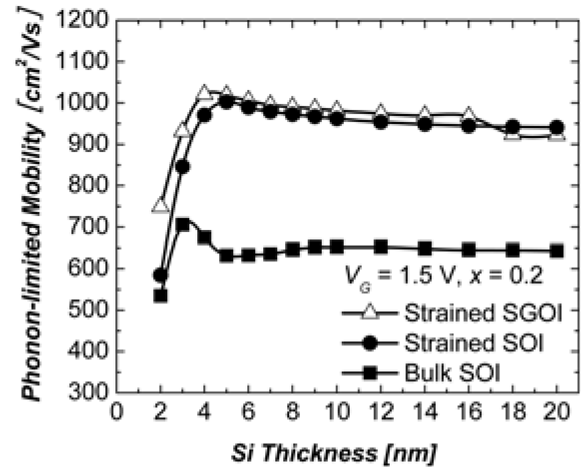


Fig. 7. Phonon-limited electron mobility dependency on the strained Si thickness in an SGOI n-MOSFET.

electron mobility in an sSOI n-MOSFET with that in an SGOI n-MOSFET as function of the strained Si thickness. We observed that in the Si thickness range from 10 nm down to 3 nm, the phonon-limited electron mobility in the sSOI n-MOSFET was about 1.5 times higher than that in a conventional SOI n-MOSFET. In addition, we have shown for the first time that the electron mobility in the sSOI n-MOSFET was about 3.2% higher than that in the sSOI n-MOSFET. We attribute this to two physical phenomena: (i) the sSOI n-MOSFET has higher inter-valley scattering rates than does the SGOI n-MOSFET, because of the greater carrier confinements, and (ii) some electrons in the inversion layer of the SGOI n-MOSFET tunnel into the SiGe layer.

In conclusion, we suggest that device and circuit designers should consider the trade-off involving in applying sSOI n-MOSFET technology; a 3.2% lower enhancement in the electron mobility, as compared to an increased production yield. Furthermore, further experiments should be conducted to analyze this issue.

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