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Strained silicon substrate technologies for enhancement of transistor performance

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Strain-induced improvement of electron or hole mobility is a very attractive way of enhancing the speed performance of integrated circuits in addition to device scaling. This paper reviews several promising substrate technologies for the exploitation of strain-induced effects. Strained silicon substrates incorporating layer structures such as strained-Si on a relaxed SiGe buffer layer, strained-Si-on-insulator, and strained-Si/SiGe-on-insulator, are examined. Technical challenges for these substrate technologies are investigated, and their relative merits are compared.

Key words: Strain, transistor, CMOS, substrate.

Introduction

Scaling of complementary metal-oxide-semiconductor (CMOS) transistors faces many challenges related to physical limitations. An emerging industry trend is the exploration of alternative ways to enhance CMOS transistor performance in addition to device scaling. One of the most promising ways makes use of strain-induced improvement in electronic properties. Beneficial effects such as increase in carrier mobility can be realized, paving the way for even faster integrated circuits. Such a strain-induced mobility enhancement phenomenon will be increasingly exploited for improving integrated circuit performance.

Semiconductor manufacturers currently use epitaxial silicon (Si) wafers, polished Si wafers, or silicon-on-insulator wafers as the starting materials for integrated circuit fabrication. These conventional substrates are usually strain-free. With the emergence of strain as an additional parameter for improving transistor performance, it is interesting to introduce strain in semiconductor substrates prior to the CMOS fabrication process. In this paper, we review several promising substrate technologies for the exploitation of strain-induced effects. These substrate technologies make use of recent advances in epitaxy, wafer bonding, or wafer separation techniques. Several new and novel epitaxial substrate designs that may be used for advanced and future semiconductor applications will be discussed.

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Strain and Mobility Enhancement

For high performance logic applications, the International Technology Roadmap for Semiconductors (ITRS) [1] projected that the mobility enhancement is 30%, 70%, and 100% in the years 2010, 2013, and 2016, respectively, as shown in Fig. 1. Even for low operating power applications, mobility enhancements of up to 70% are required in the year 2016. In order to realize such a high mobility enhancement, the required strain level in the substrate is significant.

According to Fig. 2, the required tensile strain for achieving 50% enhancement of electron and hole mobility can be as large as 0.5% and 1.0%, respectively. In general, if biaxial tensile strain is used, holes require a larger strain to achieve the same mobility enhancement. An illustration of biaxial tensile strain in the silicon lattice is shown in Fig. 3. This strain is typically induced in the topmost layer of the substrate where the inversion layer of the transistor resides.

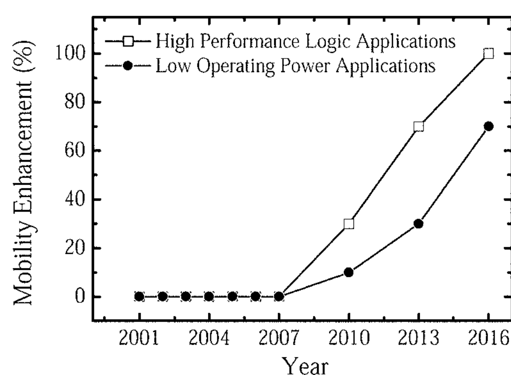

Fig. 1. Projection of mobility enhancement according to International Technology Roadmap for Semiconductors (ITRS) 2001 [1].

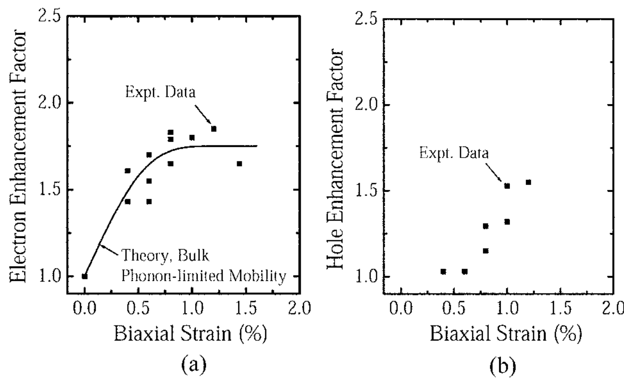

Fig. 2. Relation between (a) electron and (b) hole mobility enhancement and biaxial tensile strain in the silicon substrate. The theoretical bulk mobility for electrons is also plotted [2].

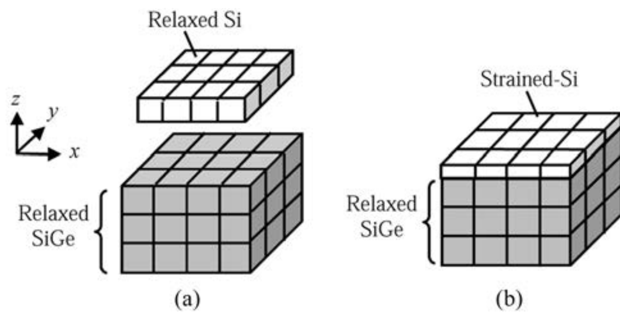

Fig. 3. The lattice constant of (a) relaxed Si is stretched in the x and y directions to result in biaxial tensile strain in (b) strained Si.

Strained Substrates

Bulk Substrates

To introduce biaxial tensile strain in a silicon layer, it has to be epitaxially grown on a crystalline surface with a larger lattice constant, e.g. a relaxed SiGe buffer layer [2, 3]. Figure 4 shows an example of a bulk strained Si substrate design. A $Si_{1-x}Ge_x$ graded buffer layer is grown on a substrate where the Ge mole fraction is graded from 0 to x. A relaxed $Si_{1-x}Ge_x$ layer is formed on the graded buffer, followed by a silicon layer. Since the lattice constant of silicon is smaller than that of relaxed SiGe, the silicon layer experiences a biaxial tensile strain in the plane of the substrate, leading to enhanced carrier transport properties. Transi-

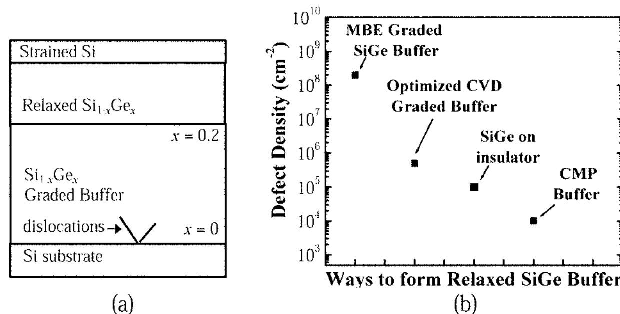

Fig. 4. (a) Schematic of strained Si substrate design, and (b) defect reduction in strained-Si on relaxed-SiGe substrates.

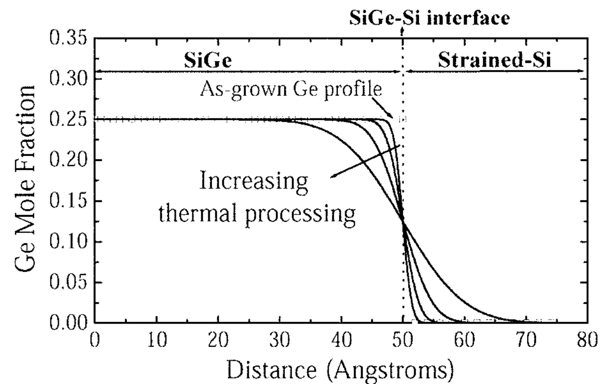

Fig. 5. Ge diffusion into the strained Si layer increases with increasing thermal budget. In this example, a $Si_{0.75}Ge_{0.25}$ buffer layer is used.

stors formed on the strained Si layer have enhanced carrier mobility and speed performance. Strain and mobility enhancement can be increased by increasing the Ge content in the relaxed SiGe buffer layer.

There are several challenges to be overcome for the strained Si substrate. For example, dislocations propagating from crystalline-mismatched interfaces result in the formation of defects in the vicinity of the wafer surface. Though the defect density has been significantly reduced (Fig. 5), the defect density is still several orders of magnitude higher than that of conventional substrates. Another challenge relates to process integration. The strained Si layer has to be kept thin to prevent relaxation of the strain. However, thermal processing results in diffusion of Ge from the relaxed SiGe layer into the strained Si layer, degrading gate dielectric interface properties and carrier mobility [4]. The thermal budget of the process flow must be kept very low to alleviate this problem. An additional requirement for such a substrate could relate to the sharpness of the Si/SiGe heterojunction. The widespread adoption of novel epitaxial substrates depends on the existence of cost-effective solutions and the overcoming of the above mentioned technical difficulties.

Semiconductor-on-Insulator Substrates

Strained-Si can also be grown on a relaxed SiGe layer that is formed on an insulator layer [5], as shown in Fig. 6(a), to combine the advantages of strained-Si and SOI. A bulk substrate underlies the insulator layer. The relaxed SiGe layer may be formed by a wafer bonding and separation technique, a Ge condensation technique, or a SIMOX technique. The cost of this substrate is lower than that for the bulk strained silicon approach. However, problems associated with Ge diffusion to the gate dielectric interface remain.

To eliminate this problem, the strained Si layer is formed directly on an insulator layer [6], as shown in Fig. 6(b). This can be done by a wafer bonding and separation technique to transfer a layer of strained silicon from a donor wafer (e.g. a bulk strained-Si

Table 1. Comparison of Strained Substrate Technologies

	Ge Diffusion	Defect Formation	Device Integration	Cost
strained-Si/SiGe/bulk-Si	–	– –	– –	– –
strained-Si/SiGe/insulator	–	–	–	–
strained-Si/insulator	+	+	+	+

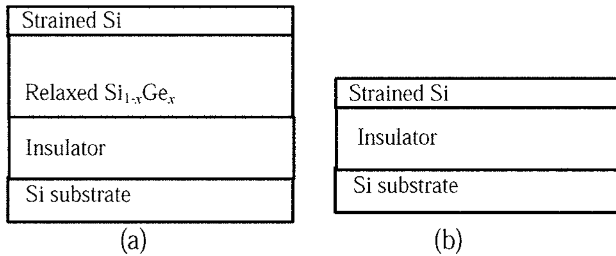

Fig. 6. Schematic of (a) strained-Si/SiGe/insulator substrate, and (b) strained-Si/insulator substrate.

substrate) to a target wafer with an insulator surface. The strained-Si-on-insulator (SSOI) substrate thus formed is immune to Ge diffusion problems, is not prone to misfit dislocation formation at strained Si-SiGe interfaces, has less device integration issues, and has a lower cost of manufacture. Table 1 compares the strained-silicon substrate technologies discussed.

Conclusions

Several existing strained silicon substrate technologies have been reviewed and compared. Strained silicon substrate is a very promising way to provide transistor performance enhancement required by the ITRS. A strained-Si-oninsulator substrate appears to be the best candidate for this application.

References

1. International Technology Roadmap for Semiconductors (ITRS) 2001, Semiconductor Industry Association, 2001.
2. J. Welser, J.L. Hoyt, S. Takagi, and J.F. Gibbons, “Strain dependence of the performance enhancement in strained-Si nMOSFETs,” IEDM (1994) 373-376.
3. K. Rim, J.L. Hoyt, and J.F. Gibbons, “Fabrication and analysis of deep submicron strained-Si NMOSFETs,” IEEE Trans. Elect. Dev. 47 (2000) 1406-1415.
4. M.T. Currie, C.W. Leitz, T.A. Langdo, G. Taraschi, E.A. Fitzgerald, and D.A. Antoniadis, “Carrier mobilities and process stability of strained Si n- and p-MOSFETs on SiGe virtual substrates,” J. Vac. Sci. Tech. B19 (2001) 2268-2279, 2001.
5. T. Mizuno, N. Sugiyama, A. Kurobe, and S. Takagi, “Advanced SOI p-MOSFETs with strained-Si channel on SiGe-on-insulator substrate fabricated by SIMOX technology,” IEEE Trans. Elect. Dev. 48 (2001) 1612-1618.
6. T.A. Langdo, A. Lochtefeld, M.T. Currie, R. Hammond, V.K. Yang, J.A. Carlin, C.J. Vineis, G. Braithwaite, H. Badawi, M.T. Bulsara, and E.A. Fitzgerald, “Preparation of novel SiGe-free strained Si on insulator substrates,” IEEE SOI Conf. Oct. (2002) 211-212.