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Two possible ways of lowering the production cost of crystalline silicon wafers for solar cells

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Making a thinner wafer is a simple way of reducing the production costs of silicon solar cells. However, supporting this thin wafer in some way is necessary to protect the solar cell from breakage. A cheap substrate needs to be developed and attached to the thin silicon solar cell with aluminum paste. Silicon solar cells of 150 μm thickness with a sintered substrate on the back side show a 5.4% conversion efficiency as a solar cell. Compared to commercial silicon cells, a lower short circuit current (Jsc) is obtained. This might be due to the poor conduction in the back layer of aluminum which is absorbed into the supporting substrate during the annealing for bonding. Another way of lowering wafer costs is to apply the extrinsic gettering method to the silicon wafers made from cheap silicon raw materials which possibly contain metal impurities. Damage induced during the slicing process of the silicon wafers with wire saws is found to generate dislocations after the oxidation process which may contribute to the gettering. Therefore, without any additional process, cheaper raw materials are expected to be used for the cost reduction of the silicon wafers.

Key words: saw damage, gettering, bonding, solar cell.

Introduction

The enhancement of conversion efficiency and the reduction of production costs are the two main research areas in the production of the crystalline silicon solar cells. The cost of silicon wafers typically accounts for more than 65% of the total production costs of a silicon solar cells [1]. To make the crystalline silicon a competitive material for solar cells, lowering the wafer cost is highly desirable. One way of lowering the wafer cost is by reducing the thickness of the silicon wafer. Currrently, wafers thicker than 350 μm are used for producing solar cells. Including 250 μm of kerf loss, 600 μm of silicon needs to be used in order to make a wafer of 350 μm. Recently, slicing technology has been improved enabling to cut the silicon wafers to 150 μm thickness. With this advance, a 47% yield increase is expected. However, thin wafers are easily broken during the fabrication process. To avoid this breakage problem, the careful handling of wafers is vitally important. A non-contact fabrication process can be one solution. Another solution is to support thin wafers with a cheap substrate. This supporting substrate should not only be strong but also have a thermal expansion coefficient similar to silicon. If there is a big difference in the thermal expansion coefficient between these two materials, then another breakage problem can occur. The breakage may occur during fabrication, or the solar cell may fail in the field. One way to make the supporting substrate cheaper is to use cheaper raw materials. Fortunately, during the slicing process of the silicon wafers, silicon saw dust is collected in the form of sludge. This sludge is composed of silicon powder of 6 μm in diameter. If properly treated, this material can be a good raw material for a cheap substrate. In this investigation, a thin solar cell made from a 150 μm thickness wafer was attached to the cheap substrate with aluminum paste to examine the structure as a possible way of reducing the production cost of solar cells.

Another way of reducing the wafer cost is the application of the gettering phenomena, in which some structural defects are known to absorb the metal impurities present in the silicon crystal [2]. For semiconductor applications, several methods of gettering have been developed. One of the most popular ones is by wet blasting with silica slurry on the back side of the silicon wafer. For the solar cell application, aluminum and phosphorous gettering is currently under investigation [3]. In addition to these techniques, extrinsic gettering by mechanical damage might be a preferable method. The mechanical damage induced due to sawing seems greater than the damage induced by wet blasting with silica slurry. In this investigation, oxidation of the silicon wafer sliced with a wire saw is conducted to test this as a possible method of gettering.

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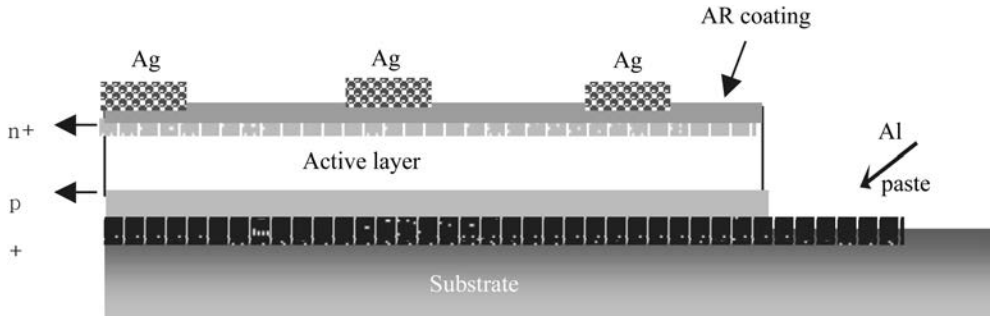

Fig. 1. Bonded solar cell structure.

Experiments

Thin solar cell bonded to cheap substrate

For the thin silicon solar cell structure as in Fig. 1, silicon wafers of p-tpye <100> were etched to a thickness of 150 μm with KOH solution. Then, an emitter was formed on this wafer by annealing at 950 °C for 30 minutes with $POCl_3$. A TiO_2 layer on the top of the emitter layer was formed with APCVD (Atmospheric Pressure Chemical Vapor Deposition). With screen printing techniques, the aluminum layer is printed on the back side of the wafer.

Due to its abundance, silicon sludge produced during the slicing process of silicon wafers has been selected as the material for the back supporting substrate of thin solar cells. The average size of the silicon powder in the sludge is 6 μm. With attrition milling, the average size of the silicon powder was ground to 1 μm. Aluminum powder was added to this powder as a binder for sintering. Sintering was conducted at 1200 °C for three hours. The strength of this sintered stock was measured with a three point bend tester. In addition, the thermal expansion coefficient was measured with a thermo mechanical analyzer (TMA) to determine the thermal matching with the thin silicon solar cell attached on the top of this back support.

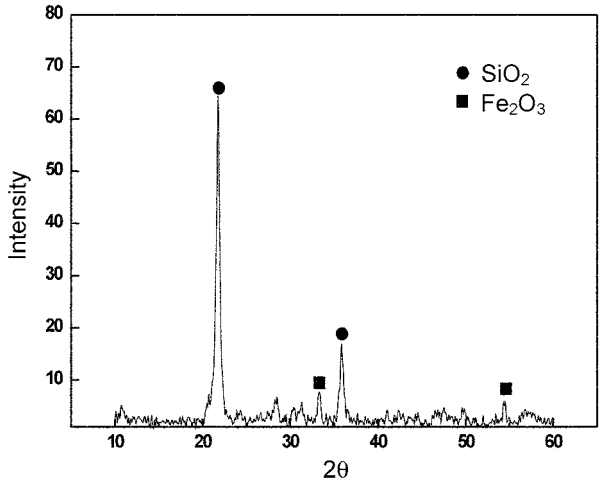

Fig. 2. X-ray diffraction pattern of sintered substrate.

Gettering with saw damage-induced defects

Silicon crystals were sliced into wafers with a wire saw machine. The diameter of the SiC slurry used in this process was 8 μm on average. For the generation of the defects due to the saw damage, wafers were wet-oxidized with a tube furnace. The oxidation was conducted at 1100 °C for 2 hours. After stripping off the oxide with HF solution, the surface of the wafer was etched with Wright's solution for defect delineation. Afterwards, an examination of the defects was conducted with an optical microscope and scanning electron microscope (SEM).

Results and Discussion

Thin solar cell bonded to cheap substrate

Figure 2 shows the X-ray diffraction (XRD) pattern of the sintered stock made of silicon sludge and aluminum. As can be seen, since the sintering was conducted in an oxygen ambient, SiO_2 and Fe_2O_3 are the main components in the sintered stock. This Fe_2O_3 is believed to be produced by steel balls used in the attrition milling process. Since the silicon powder is harder than the steel balls, large portions of the steel balls are worn away during the milling process. During sintering in the oxygen ambient, most of steel debris is then converted into Fe_2O_3. However, Al_2O_3 is not found in a subsequent X-ray diffraction analysis despite the fact that the powder mixture uses 5 wt% of aluminum as bonding material. During sintering, aluminum might absorb the silicon to form aluminum silicide first, then SiO_2 is formed from the aluminum silicide during further oxidation as proposed previously [4]. It was found that the material sintered in an inert atmosphere such as argon shows very little strength and can not be used as a back supporting substrate. Figure 3 shows the strength of the sintered materials as a function of the sintering temperature. As can be seen in the figure, the material containing 5 wt% aluminum shows a strength higher than 0.45 MPa when sintered at 1200 °C. Since the silicon crystal itself shows a strength of 0.25 MPa, the silicon sludge and aluminum mixture is believed to have enough strength to be a back supporting substrate of thin silicon solar cells. The thermal expansion

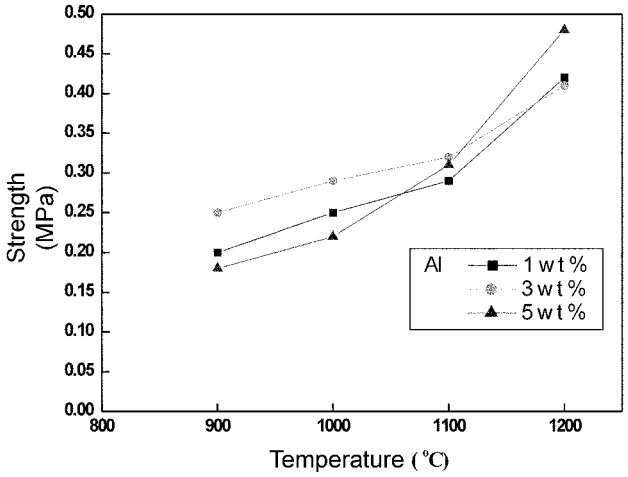

Fig. 3. Strength of sintered substrate with various Al wt% as a function of sintering temperature.

Table 1. Thermal expansion coefficient of the substrate measured by TMA at 950 °C

Specimen	Al 1 wt%	Al 3 wt%	Al 5 wt%
Thermal expansion coefficient	7.9×10^{-6}/K	8.12×10^{-6}/K	8.2×10^{-6}/K

coefficient of this material was measured with thermo mechanical analyzer (TMA) and listed in Table 1. The values are very close to 8.0×10^{-6}/K, which is the thermal expansion coefficient of a silicon crystal. From these measurements, it is believed that the silicon and aluminum mixture can be a good candidate for the back supporting substrate.

Figure 4 shows the I-V characteristics of thin solar cells bonded to the sintered substrate. As can be seen, the efficiency is lower than normal commercial solar cells. This is attributed to the poor short circuit current (Jsc) which is due to the aluminum conductor located between the thin active cell and back substrate. During the annealing at 850 °C for bonding the two layers, it was found that a large amount of aluminum is absorbed

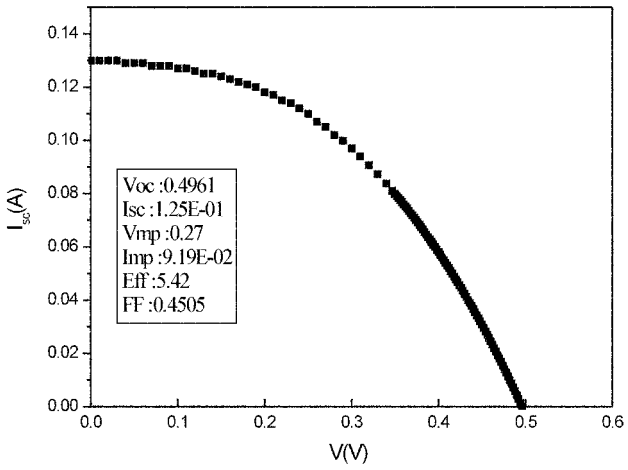

Fig. 4. I-V curve of the solar cell bonded to sintered substrate.

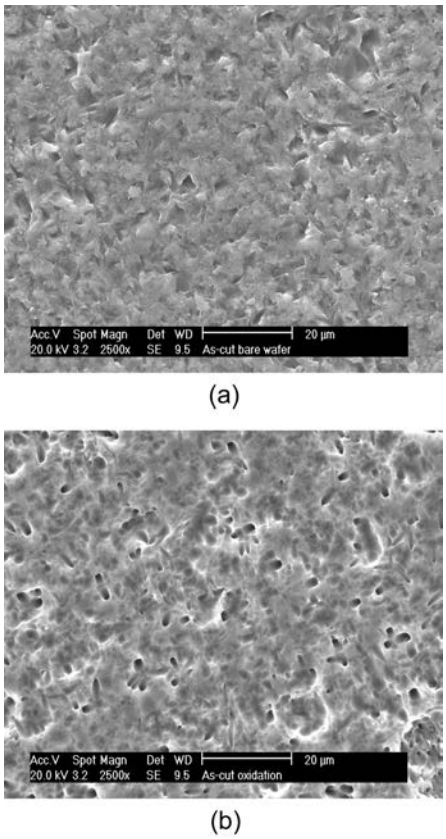

Fig. 5. SEM image of as-cut wafer (a) before (b) after wet oxidation 1100 °C for 2 hours (Wright etching 5 minutes).

into the back substrate which has a high porosity. To achieve better conversion efficiency of this cell, some kind of diffusion barrier between the aluminum layer and sintered back supporting substrate is needed.

Gettering with saw damage-induced defects

Figure 5 shows an SEM micrograph taken of the silicon surface sliced with a wire saw. A high density of etch pits can be seen in the wafer oxidized at 1100 °C for two hours. Since these etch pits are not found in the silicon wafers not oxidized, most of these etch pits are believed to be formed during oxidation. And also, most of the etch pits form dipoles without connecting lines. It is well-known that oxidation-induced stacking faults (OISF) in the etched silicon crystal appears as etch pit dipoles with etch line connecting the two etch dipoles [5]. This is due to Frank-type dislocations loops containing stacking faults inside. However, as can be seen in Fig. 5, etch pit dipoles didn't have any etch lines connecting the two dipoles. This observation indicates that the etch pit dipoles might be due to the perfect dislocation loops of 1/2<110> type. The OISF are found to be formed during the oxidation treatment of damaged silicon crystal. The amount of damage induced by the sawing might be much larger than the damage induced by silica wet blasting employed to give OISF in the silicon wafer production. It seems that the type

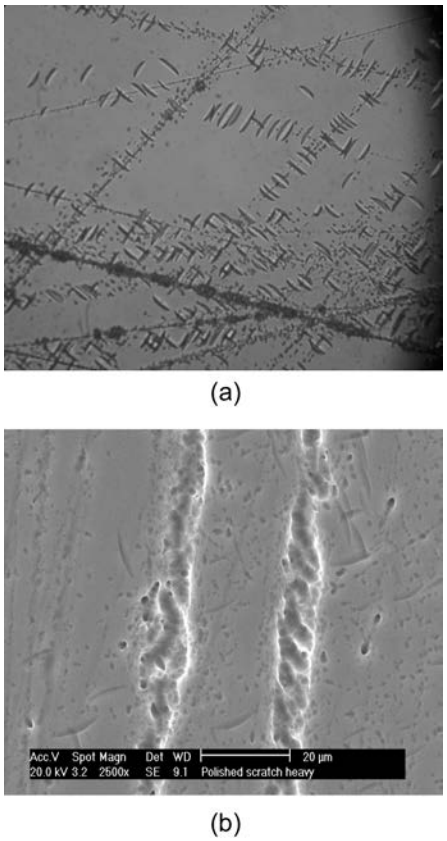

Fig. 6. Oxidized surface of the silicon wafer scratchd with SiC paper (a) optical microscope (b) SEM (Wright etching 5 minutes).

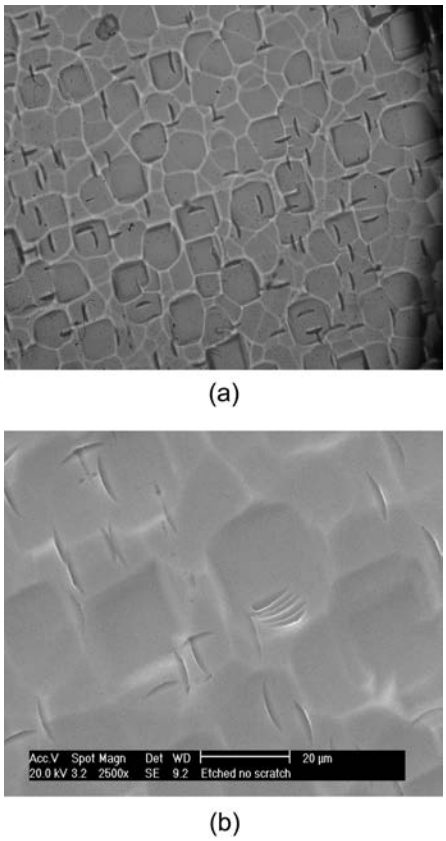

Fig. 7. Oxidized back surface silicon wafer. After lapping, surface was etched with KOH solution followed by wet blasting with silica slurry (a) optical microscope (b) SEM (wright etching 5 minutes).

of defects, whether perfect dislocation loop or stacking faults loop formed during the oxidation treatment, depend on the amount of damage left in the silicon crystal before oxidation. To clarify this assumption, polished silicon wafers are selected. Scratches are then administered to this polished surface with SiC paper. Thermal oxidation and preferential etching follow. Figure 6 is the picture taken by the optical microscope on the polished silicon surface which had scratches made by SiC paper. As can be seen in the picture, stacking faults are generated along the scratches. An interesting fact observed in this picture is that the etch pits due to the stacking faults are present along the weak scratches and etch pits which are possibly due to dislocations, are present along the heavy scratches. This observation might indicate that the generation of dislocations needs some critical value of mechanical damage. Below this critical value, stacking faults are formed. Figure 7 is micrographs taken on a specimen which has silica wet blasting damage. Without scratching, only stacking faults are formed as can be seen in Fig. 7.

The damage-induced-dislocation loops generated during the oxidation treatment are expected to work as a gettering source to lower the content of metal impurities which might be present in the cheap raw material.

Conclusions

Two possible ways of lowering the cost of silicon wafer have been described.

(1) 150 μm thin silicon solar cell bonded to a back supporting substrate was fabricated. This structure was strong enough to avoid the breakage problem of thin cells. The back supporting substrate can be prepared by sintering silicon sludge and aluminum. In this way, a cost reduction can be realized with a thinner silicon cell and a cheaper substrate prepared from silicon sludge.

(2) The wire sawing process leaves mechanical damage on each side of the wafers. This damage could induce dislocation generation during the wet oxidation process. It was observed that the type of defects depend on the amount of damage: small damage induces stacking faults and large damage induces dislocation loops during oxidation process.

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References

1. J.F. Nijs, J. Szlufcik, J. Poortmans, S. Sivoththaman and P. Mertens, IEEE Transactions on Electron Devices, Vol. 46, No. 10, October 1999.
2. F. Shimura, “Semiconductor Silicon Crystal Technology”, Academic Press, Inc, (1989) pp. 346-347.
3. I. Perichaud, Solar Energy Materials & Solar Cells 72 (2002) pp. 315-326.
4. J.E. Lawrence, Trans. Metall. Soc. AIME 242 (1968) pp. 484-489.
5. D'Heurle, F.M., A. Cros, R.D. Frrampton, and E.A. Irene, Philes Mag. B 55[2] (1987) 291.